

MAXIM
660ns μ P-Compatible,
8-Bit ADC with Track/Hold

General Description

The MX7821 high-speed, microprocessor-compatible (μ P), 8-bit analog-to-digital converter (ADC) is a plug-in upgrade for the industry-standard 7820. The MX7821 uses a half-flash technique, resulting in a 660ns conversion time vs. 1.36 μ s for the 7820. A V_{SS} pin, not supplied by the 7820, supports dual power supplies and bipolar analog inputs.

The MX7821 has track-and-hold function capable of digitizing a 100kHz signal, and is tested for both its static and dynamic capability. The converter- μ P interface appears as a memory location or input/output port that requires no external interface logic. The data outputs use latched, three-state buffered circuitry for direct connection to a μ P data bus or system input port. The MX7821 has an overflow output for cascading devices to attain higher resolution. The ADC's input/reference arrangement enables ratiometric operation. For a detailed description of MX7821 operation, refer to the MX7820 data sheet.

Applications

Digital-Signal Processing
High-Speed Data Acquisition
Telecommunications
High-Speed Servo Loops
Audio Systems

Features

- ◆ 660ns Conversion Time
- ◆ 20-Pin Narrow DIP Package
- ◆ No External Clock
- ◆ Pin-Compatible Upgrade for Industry-Standard 7820
- ◆ 100kHz Input Signal Bandwidth
- ◆ Bipolar/Unipolar Inputs
- ◆ Single +5V or Dual $\pm 5V$ Supplies
- ◆ Ratiometric Reference Inputs
- ◆ Static and Dynamic Tested
- ◆ Internal Track/Hold

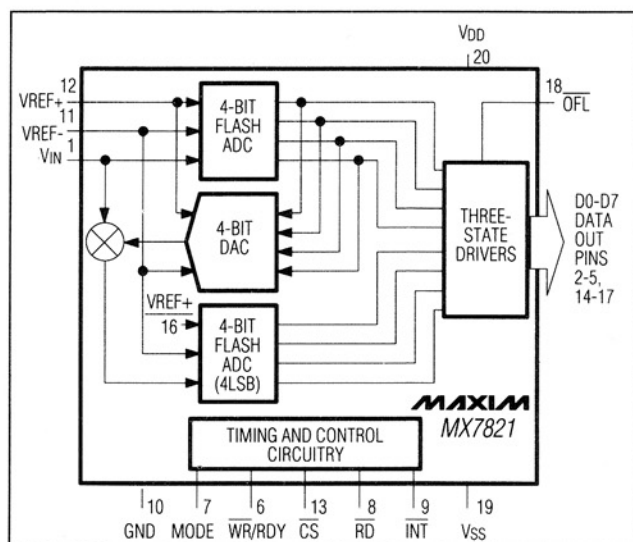
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MX7821KN	0°C to +70°C	20 Plastic DIP
MX7821KR	0°C to +70°C	20 Wide SO
MX7821KP	0°C to +70°C	20 PLCC
MX7821K/D	0°C to +70°C	Dice*
MX7821BQ	-40°C to +85°C	20 CERDIP
MX7821KEWP	-40°C to +85°C	20 Wide SO
MX7821TE	-55°C to +125°C	20 LCC**
MX7821TQ	-55°C to +125°C	20 CERDIP**

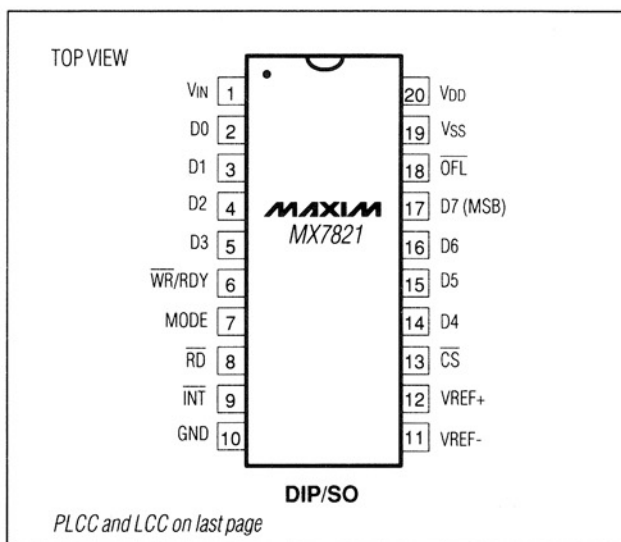
* Contact factory for dice specifications.

**** Contact factory for availability and processing to MIL-STD-883.**

Functional Diagram



Pin Configurations



MX7821

660ns μ P-Compatible, 8-Bit ADC with Track/Hold

ABSOLUTE MAXIMUM RATINGS

VDD to GND	-0.3V to +7V
VSS to GND	+0.3V to -7V
Digital Output Voltage to GND (Pins 2-5, 9, 14-16, 18)	-0.3V to VDD +0.3V
VREF+ to AGND	VSS -0.3V to VDD +0.3V
VREF- to AGND	VSS -0.3V to VDD +0.3V
VIN to GND	VSS -0.3V to VDD +0.3V
Continuous Power Dissipation (any package) to +75°C	1000mW
derate above +75°C by	10mW/°C

Operating Temperature Ranges:

MX7821K	0°C to +70°C
MX7821B	-40°C to +85°C
MX7821T	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10 sec)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VDD = +5V $\pm$ 5%; GND = 0V; Unipolar Input Range: VSS = 0V, VREF+ = 5V, VREF- = 0V; Bipolar Input Range: VSS = -5V $\pm$ 5%, VREF+ = 2.5V, VREF- = -2.5V; specifications apply for RD mode, Pin 7 = 0V; TA = TMIN to TMAX, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UNIPOLAR INPUT RANGE						
Resolution	N		8			Bits
Total Unadjusted Error (Note 2)	TUE				± 1	LSB
No Missing Codes Resolution			8			Bits
BIPOLAR INPUT RANGE						
Resolution	N		8			Bits
Zero-Code Error					± 1	LSB
Full-Scale Error					± 1	LSB
Signal-to-Noise Ratio	SNR	VIN = 99.85kHz full-scale sine wave with fSAMPLING = 500kHz	45			dB
Total Harmonic Distortion	THD	VIN = 99.85kHz full-scale sine wave with fSAMPLING = 500kHz			-50	dB
Peak Harmonic or Spurious Noise		VIN = 99.85kHz full-scale sine wave with fSAMPLING = 500kHz			-50	dB
Intermodulation Distortion	IMD	fa(84.72kHz) and fb(94.97kHz) full-scale sine waves with fSAMPL- ING = 500kHz	2nd-order terms		-50	dB
			3rd-order terms		-50	
Slew Rate, Tracking				2.36	1.6	V/ μ s
REFERENCE INPUT						
Input Resistance		Resistance between VREF+ and VREF-	1		4	k Ω
VREF+ Input Range			VREF-		VDD	V
VREF- Input Range			VSS		VREF+	V
ANALOG INPUT						
Input Voltage Range			VREF-		VREF+	V
Input Leakage Current		-5V $\leq$ VIN $\leq$ 5V			± 3	μ A
Input Capacitance	CIN			32		pF

660ns μ P-Compatible, 8-Bit ADC with Track/Hold

MX7821

ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = +5V \pm 5\%$; $GND = 0V$; Unipolar Input Range: $V_{SS} = 0V$, $V_{REF+} = 5V$, $V_{REF-} = 0V$; Bipolar Input Range: $V_{SS} = -5V \pm 5\%$, $V_{REF+} = 2.5V$, $V_{REF-} = -2.5V$; specifications apply for RD mode, Pin 7 = 0V; $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS						
Input High Voltage	V_{INH}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$	2.4			V
		MODE	3.5			
Input Low Voltage	V_{INL}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$			0.8	V
		MODE			1.5	
Input High Current	I_{INH}	$\overline{CS}$, $\overline{RD}$			1	μA
		$\overline{WR}$			3	
		MODE		50	200	
Input Low Current	I_{INL}				-1	μA
Input Capacitance (Note 3)	C_{IN}			5	8	pF
LOGIC OUTPUTS						
Output Low Voltage	V_{OL}	D7-D0, $\overline{INT}$, $\overline{OFL}$; $I_{SINK} = 1.6mA$			0.4	V
		RDY; $I_{SINK} = 2.6mA$			0.4	
Output High Voltage	V_{OH}	D7-D0, $\overline{INT}$, $\overline{OFL}$; $I_{SOURCE} = -360\mu A$	4.0			V
Floating State Leakage Current	I_{LKG}	D7-D0, RDY			± 3	μA
Floating State Output Capacitance (Note 3)	C_{OUT}	D7-D0, RDY		5	8	pF
POWER REQUIREMENTS						
Supply Current	I_{DD}	$CS = RD = 0V$	MX7821K		15	mA
			MAX7821B/T		20	
	I_{SS}				100	μA
Power Dissipation	P_D			50		mW
Power-Supply Sensitivity	PSR	$V_{DD} = 4.75V$ to $5.25V$, $V_{REF+} = 4.75V$ MAX for unipolar mode		$\pm 1/16$	$\pm 1/4$	LSB

Note 1: Performance over power-supply tolerance guaranteed by power-supply rejection test.

Note 2: Total Unadjusted Error includes relative accuracy, zero-code error, and full-scale error.

Note 3: Guaranteed by design.

TIMING CHARACTERISTICS

($V_{DD} = +5V$, $V_{SS} = 0V$ or $-5V$, Unipolar or Bipolar Input Range, $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ to $\overline{RD}/\overline{WR}$ Setup Time	t_{CSS}		0			ns
$\overline{CS}$ to $\overline{RD}/\overline{WR}$ Hold Time	t_{CSH}		0			ns
$\overline{CS}$ to RDY Delay (Note 4)	t_{RDY}	$T_A = +25^\circ C$			70	ns
		$T_A = T_{MIN}$ to T_{MAX}			85	
					100	
Conversion Time (RD Mode)	t_{CRD}	$T_A = +25^\circ C$			700	ns
		$T_A = T_{MIN}$ to T_{MAX}			875	
					975	

660ns μ P-Compatible, 8-Bit ADC with Track/Hold

TIMING CHARACTERISTICS (continued)

($V_{DD} = +5V$, $V_{SS} = 0V$ or $-5V$, Unipolar or Bipolar Input Range, $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data-Access Time (RD Mode) (Note 5)	t_{ACC0}	$T_A = +25^\circ C$, $C_L = 20pF$			$t_{CRD}+25$	ns
		$T_A = T_{MIN}$ to T_{MAX} , $C_L = 20pF$			$t_{CRD}+30$	
					$t_{CRD}+35$	
		$T_A = +25^\circ C$, $C_L = 100pF$			$t_{CRD}+50$	
		$T_A = T_{MIN}$ to T_{MAX} , $C_L = 100pF$			$t_{CRD}+65$	
					$t_{CRD}+75$	
$\overline{RD}$ to $\overline{INT}$ Delay (RD Mode)	t_{INTH}	$T_A = +25^\circ C$, $C_L = 50pF$		50	80	ns
		$T_A = T_{MIN}$ to T_{MAX} , $C_L = 50pF$			85	
					90	
Data-Hold Time (Note 6)	t_{DH}	$T_A = +25^\circ C$			60	ns
		$T_A = T_{MIN}$ to T_{MAX}			70	
					80	
Delay Time Between Conversions	t_p	$T_A = +25^\circ C$	350			ns
		$T_A = T_{MIN}$ to T_{MAX}				
Write Pulse Width	t_{WR}	$T_A = +25^\circ C$	0.250		10	μs
		$T_A = T_{MIN}$ to T_{MAX}				
Delay Time Between WR and RD Pulses	t_{RD}	$T_A = +25^\circ C$	250			ns
		$T_A = T_{MIN}$ to T_{MAX}				
$\overline{RD}$ Pulse Width (WR-RD Mode) Determined by t_{ACC1}	t_{READ1}	$T_A = +25^\circ C$ (Figure 3)	160			ns
		$T_A = T_{MIN}$ to T_{MAX} (Figure 3)				
Data-Access Time (WR-RD Mode) (Note 5)	t_{ACC1}	$T_A = +25^\circ C$, $C_L = 20pF$ (Figure 3) (Note 3)			160	ns
		$T_A = T_{MIN}$ to T_{MAX} , $C_L = 20pF$ (Figure 3) (Note 3)			205	
					240	
		$T_A = +25^\circ C$, $C_L = 100pF$ (Figure 3)			185	
		$T_A = T_{MIN}$ to T_{MAX} , $C_L = 100pF$ (Figure 3)			235	
					275	
$\overline{RD}$ to $\overline{INT}$ Delay	t_{RI}	$T_A = +25^\circ C$			150	ns
		$T_A = T_{MIN}$ to T_{MAX}			185	
					220	
$\overline{WR}$ to $\overline{INT}$ Delay	t_{INTL}	$T_A = +25^\circ C$, $C_L = 50pF$	380		500	ns
		$T_A = T_{MIN}$ to T_{MAX} , $C_L = 50pF$			610	
					700	

660ns μ P-Compatible, 8-Bit ADC with Track/Hold

MX7821

TIMING CHARACTERISTICS (continued)

(V_{DD} = +5V, V_{SS} = 0V or -5V, Unipolar or Bipolar Input Range, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RD Pulse Width (WR-RD Mode) Determined by t _{ACC2}	t _{READ2}	T _A = +25°C (Figure 4)			65	ns
		T _A = T _{MIN} to T _{MAX} (Figure 4)			75	
					85	
Data-Access Time (WR-RD Mode) (Note 5)	t _{ACC2}	T _A = +25°C, C _L = 20pF (Figure 4) (Note 3)			65	ns
		T _A = T _{MIN} to T _{MAX} , C _L = 20pF (Note 3)			75	
					85	
		T _A = +25°C, C _L = 100pF (Figure 4)			90	
		T _A = T _{MIN} to T _{MAX} , C _L = 100pF (Figure 4)			110	
WR to INT Delay (Stand-Alone Operation)	t _{IHWR}	T _A = +25°C, C _L = 50pF			80	ns
		T _A = T _{MIN} to T _{MAX} , C _L = 50pF			100	
					120	
Data-Access Time After INT (Stand-Alone Operation) (Note 5)	t _{ID}	T _A = +25°C, C _L = 20pF (Note 3)			30	ns
		T _A = T _{MIN} to T _{MAX} , C _L = 20pF (Note 3)			35	
					40	
		T _A = +25°C, C _L = 100pF			45	
		T _A = T _{MIN} to T _{MAX} , C _L = 100pF			60	
					70	

Note 3: Guaranteed by design.

Note 4: C_L = 50pF and R_L = 5k Ω pull-up resistor.

Note 5: See Figure 1 for load circuit. Parameter defined as the time required for the output to cross +0.8V or +2.4V.

Note 6: See Figure 2 for load circuit. Parameter defined as the time required for data lines to change 0.5V.

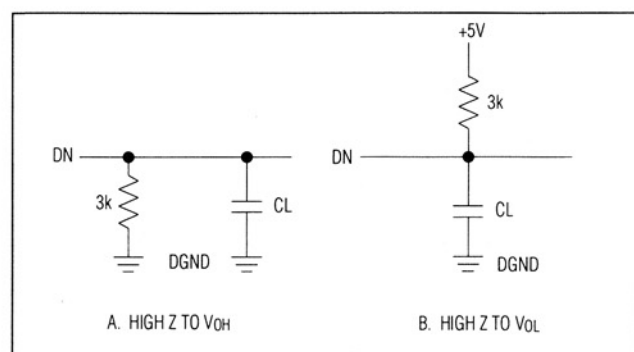


Figure 1. Load Circuits for Data-Access Time Test

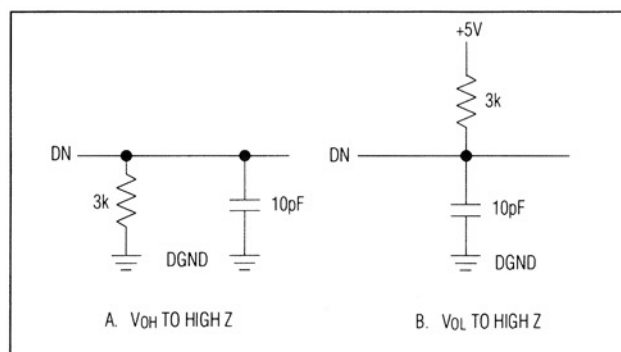


Figure 2. Load Circuits for Data-Hold Time Test

660ns μ P-Compatible, 8-Bit ADC with Track/Hold

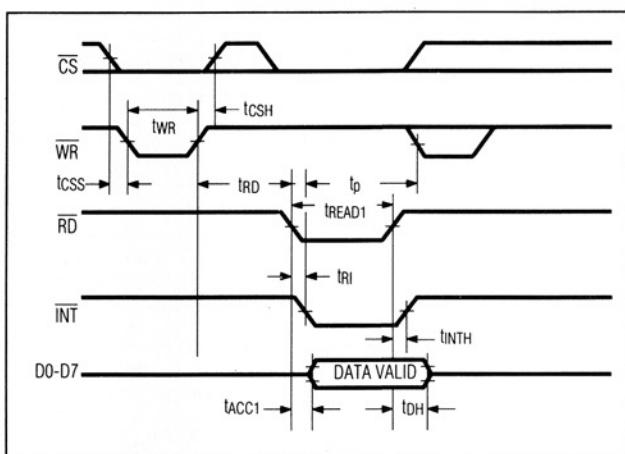


Figure 3. WR-RD Mode Timing ($t_{RD} < t_{INTL}$)

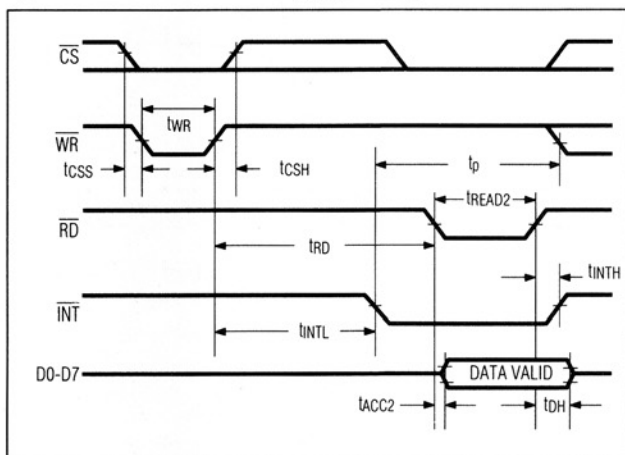


Figure 4. WR-RD Mode Timing ($t_{RD} > t_{INTL}$)

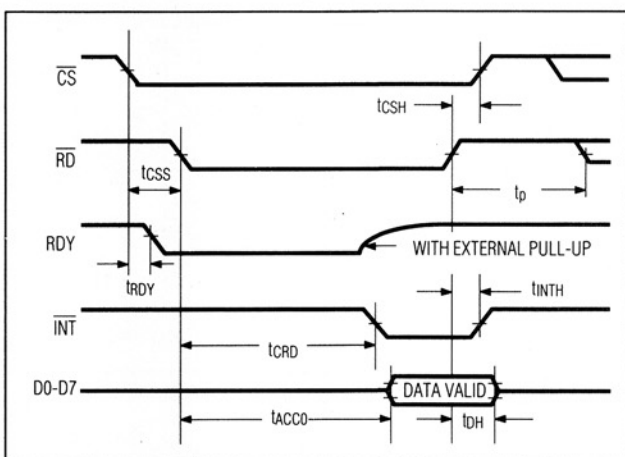


Figure 5. RD Mode

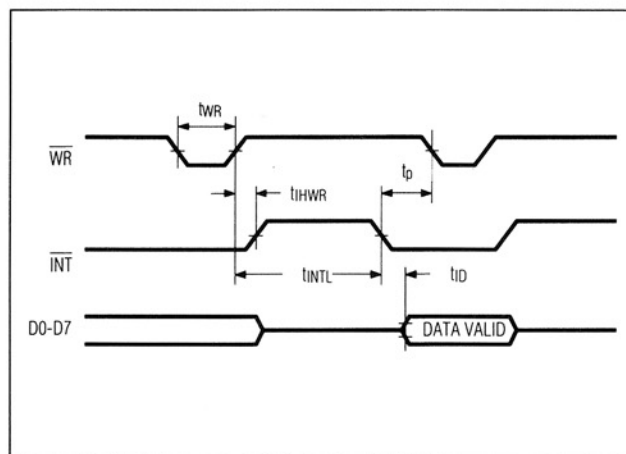
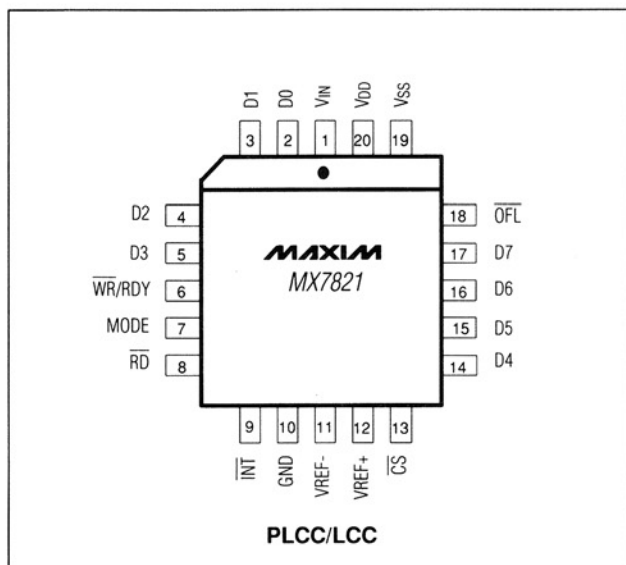


Figure 6. WR-RD Mode Stand-Alone Operation ($\overline{CS} = \overline{RD} = 0$)

Pin Configurations (continued)



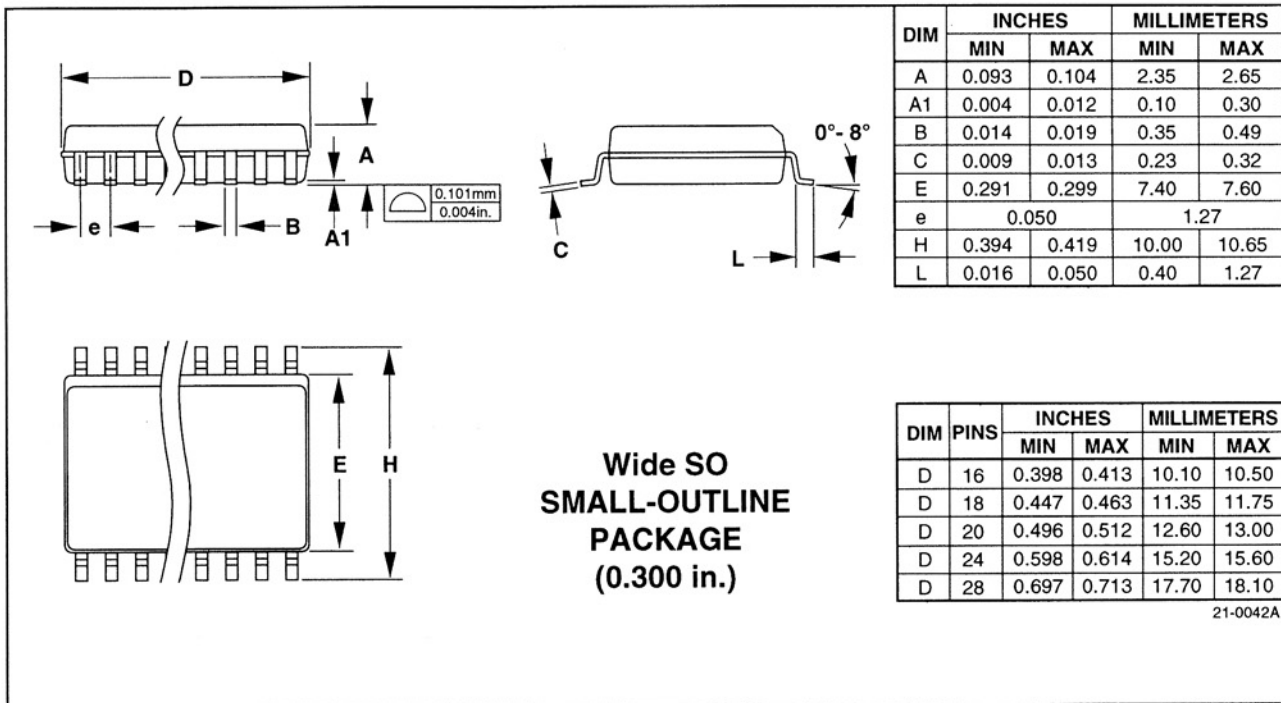
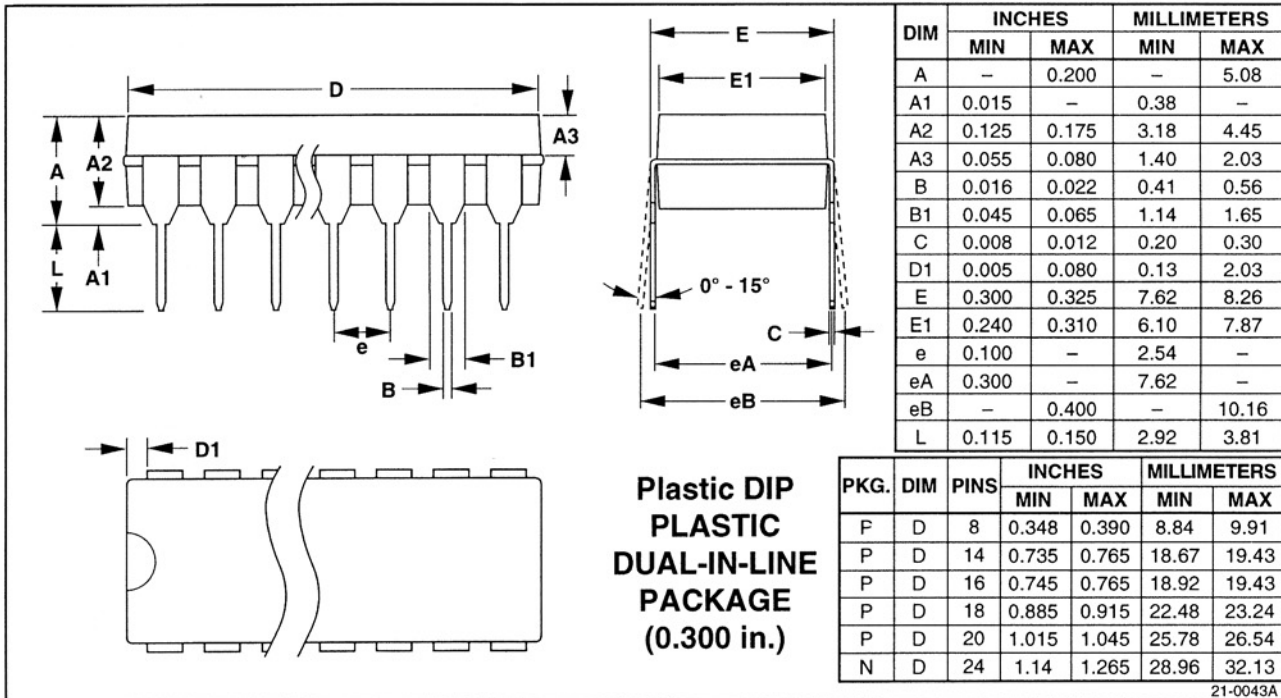
For application information, refer to the MX7820 data sheet.

660ns μ P-Compatible, 8-Bit ADC with Track/Hold

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)

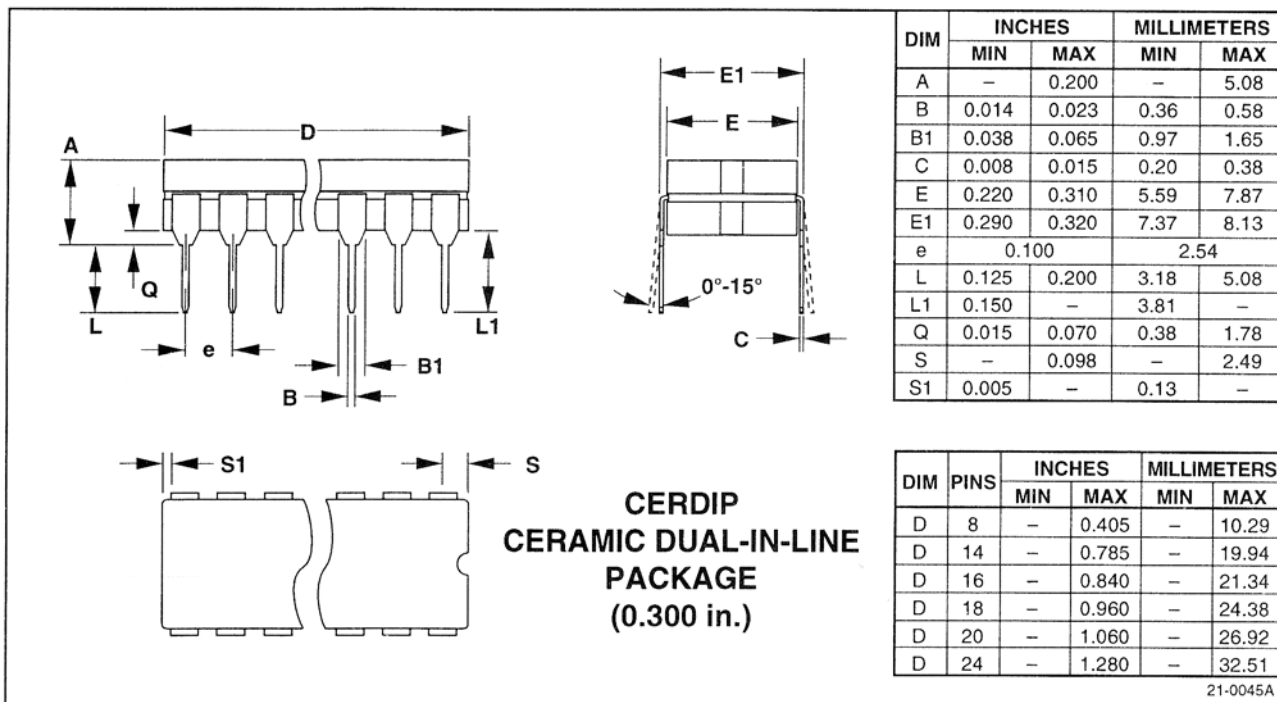
MX7821



660ns μ P-Compatible, 8-Bit ADC with Track/Hold

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

8 **Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 (408) 737-7600**